III. Remarks

A. Rejection under 35 U.S.C. §102

The Action again rejects Claims 1-2, 11, 13-14, 17 and 21-22 as being anticipated by U.S. Patent No. 6,268,633 to Pio et al. Reconsideration and withdrawal of this rejection are respectfully requested in view of the foregoing amendments and following arguments.

Independent Claim 1 has been amended to recite that the MOS device has a length and a width. It is submitted that this feature is inherent in the recitation of "MOS device," as would be understood by those in the art, and does not raise new issues for search by the Examiner. Claim 1 has also been amended to recite that the first and second source/drain regions are spaced laterally apart relative to one another "along the length of said device" in order to define the length dimension of the device relative to the source/drain regions. Further, Claim 1 has been amended to recite that the dimension of the gate claimed as being confined to be substantially within the active region of the device is substantially parallel to "the width of the device" rather than parallel to at least one of the first and second source/drain regions. This recitation of the relative orientation of the length and width of the device is described fully at Page 5, first full paragraph of the application as filed.

Similar amendments have been made to independent Claim 14 and 21.

1. Gate Feature (Claim 1)

As explained in connection with prior art FIG. 2C of the present application, "the gate 256 of traditional MOS device 250 extends beyond the active region of the device and onto the field oxide regions 264 (inactive region) of the device." This extended structure detrimentally can cause increased extrinsic gate capacitance and increased gate resistance, which are particularly harmful in high frequency applications. By confining the gate structure as claimed, this extrinsic gate capacitance and gate resistance are reduced or eliminated. (See, Application Specification, p.p. 6-7).

In the Response to Arguments section, the Examiner concludes that source and drain regions 6, 7 of Pio et al. are substantially parallel to gate 4 as shown in Figure 1 of Pio et al. The Examiner then states that Figure 2 of Pio et al. shows gate 4 is confined to be substantially within the active region of the device.

It is submitted that the amendments detailed above clarify what Applicants' mean by the recited "dimension" of the gate. With respect to the figures of Pio et al., the length of the device would be in the direction parallel to the space between regions 6 and 7 of Figure 2 and the width of the device would be generally orthogonal to length of the device and only visible from the top view of Figure 1 of Pio et al.

With this clarification, it is submitted that only FIG. 1 of Pio et al., which is a top plan view of semiconductor substrate 1, can truly illustrate whether the gate 4 of Pio et al is confined as claimed. The field oxide region (and thus the inactive region) of Pio et al. is designated by reference 12. (See, e.g., FIG. 3.). The field oxide region is not specifically labeled in the top plan view of FIG. 1, but FIGS. 2 and FIGS. 8-22 clearly show that the lateral edges of the source/drain implants 6, 7 of the device (which includes gate 4) are defined by the field oxide region 12. It is believed that the end edges of source drain regions 6, 7 (as shown in the top plan view of FIG. 1) would also be defined by the field oxide region 12.

In essence, referring to the top plan view of FIG. 1, the active region would be the generally rectangular regions 6 and 7 and the area under gate 4 that connects regions 6 and 7. All other regions of substrate 1 (except for other active regions such as device 3) would be covered by the field oxide and be "inactive", **including the significant portions of the ends of rectangular gate 4 that extend beyond regions 6 and 7 of FIG. 1**. It is submitted that these ends of the gate 4 would extend over the field oxide region 12, just as shown in Prior Art Figure 2B and 2C disclosed by Applicants in the present application. Indeed, FIGS. 6-8 show that the gate 4 is not formed until after formation of the field oxide region 12 and thus likely has portions formed over the field oxide region 12 as described above. Applicants have attempted to illustrate this point by a sketch added to FIG. 1 of Pio et al. and submitted in Exhibit A to this response.

Therefore, it is submitted that the gate 4 of Pio et al. is not "confined to be substantially within the active region of the device" in the dimension of the gate defined substantially parallel to width of the device as claimed in Claim 1.

2. Isolation Structure Feature (Claim 1)

Again, with respect to the "isolation structure" feature of Claim 1, Applicants would like to bring to the Examiner's attention the naming convention "source/drain regions" used in the application. The application provides the following:

> It is to be appreciated that, in the case of a simple MOS device, because the MOS device is symmetrical in nature, and thus bidirectional, the assignment of source and drain designations in the MOS device is essentially arbitrary. **Therefore, the source and drain regions may be referred to generally as first and second source/drain regions, respectively, where "source/drain" in this context denotes a source region or a drain region.** In a LDMOS device, which is generally not bidirectional, such source and drain designations may not be arbitrarily assigned.

Page 4, second full paragraph (emphasis added). Therefore, when Claim 1 recites that the MOS device includes "first and second source/drain regions" it recites a first source or drain region and a second source or drain region of the same device. It is further submitted that when used in the context of the claims, the recitation of "first and second source/drain regions" refers to regions of the same device (e.g., they are claimed as being part of the same "active region" in Claim 1). That the source/drain regions are part of the same device is further emphasized by the foregoing amendments, which recite that the MOS device has a length and a width and that the "first and second source/drain regions [are] spaced laterally apart relative to one another along the length of said device."

As noted above, Claim 1 recites that the MOS device (i.e., an individual transistor device) includes an isolation structure configured to isolate one or more portions of the first source/drain region from corresponding portions of the second source/drain region. As noted above, the first

source/drain region and second source/drain region **are clearly claimed as part of the same MOS device**. The Examiner cites to field oxide 12 of FIGS. 1-3 of Pio et al. as the claimed isolation structure and argues that the field oxide 12 isolates one or more portions of source/drain 6, 7 (of the first device 2) from one or more portions of the source/drain regions 8,9 (of the second device 3). As is convention, field oxide 12 is formed over substrate 1 of Pio et al. to isolate individual active regions and thus to isolate individual transistor devices, such as high voltage transistor 2 and low voltage transistor 3. Field oxide 12 is **not**, however, formed such that it isolates portions of the source and drain regions of the same MOS device as claimed in Claim 1. Therefore, it is again submitted that the isolation region identified by the Examiner, which isolates individual devices and not regions within the same device, is not "an isolation structure . . . configured to substantially isolate one or more portions of the first source/drain region from corresponding portions or the second source/drain region."

3. Summary

For at least these reasons (i.e., that Pio et al. does not recite the claimed gate and isolation region features), Claim 1 is not anticipated by and is allowable over the art of record. Claims 2-13 depend from independent Claim 1 and are, therefore, also allowable for at the least the reasons set forth for Claim 1.

Independent Claim 14 is directed to a method of forming a MOS device. The method recites the formation of substantially confined gate and isolation structures analyzed above in connection with Claim 1. For at least these reasons, Claim 14 and Claims 15-20, which depend from Claim 14, are also allowable over the art of record.

Last, Independent Claim 21 is directed to an integrated circuit including at least one MOS device where the MOS device including the substantially confined gate and isolation structures analyzed above in connection with Claim. It is submitted that Claim 21 and Claims 22-23, which depend from Claim 21, are allowable over the art of record.

Reconsideration and withdrawal of the anticipation rejections are respectfully requested.

B. Rejection under 35 U.S.C. §103

The Action rejects Claims 3-10, 12, 15-16, 18 and 20 as being obvious in view of Pio et al. and several other references. These claims depend from independent Claims 1, 14 and 21. As set forth above, these claims are allowable for at least the reasons argued for independent Claims 1, 14 and 21.

Reconsideration and withdrawal of the rejections of these claims are respectfully requested.

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IV. Conclusion

In view of the foregoing remarks and amendments, Applicant(s) submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

Dated: 11/17/05

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